CLAIMS

1. A demodulation circuit comprising:

sampling means for sampling a modulated signal;

signal synthesis means for synthesizing and holding the signals sampled by the sampling means;

polarity adjustment means for matching polarities of the signals synthesized by the signal synthesis means, with each other; and

demodulation control means for driving the sampling means to sample the modulated signal at a frequency of the modulated signal multiplied by "1/(m+0.25)" or "1/(m+0.75)" (m: 0 or natural number) and also driving the signal synthesis means to synthesize and hold the signals having phase difference "π" from each other to allow a demodulated signal to be generated by the signal synthesis means.

2. The demodulation circuit according to claim 1, wherein the polarity adjustment means supplies the modulated signal having an inverted polarity to the sampling means, thereby matching polarities of the signals synthesized by the signal synthesis means.

3. The demodulation circuit according to claim 1, wherein the polarity adjustment means inverts polarities of the signals sampled by the sampling means, thereby matching polarities of the signals synthesized by the signal synthesis means.

4. The demodulation circuit according to claim 1, wherein the demodulation control means drives the sampling means to sample the modulated signal with its polarity being inverted, thereby integrating the polarity adjustment means into the demodulation control means.

5. The demodulation circuit according to claim 1, wherein the sampling means is constituted of a unity gain sample buffer.

6. A demodulation circuit comprising:

sampling means for sampling a modulated signal;

switched capacitor filter means;

signal generation means for generating a signal on which the switched capacitor filter means performs filter processing, based on the signal sampled by the sampling means; and

demodulation control means for driving the sampling means to sample the modulated signal at a frequency of the modulated signal multiplied by "1/(m+0.25)" or "1/(m+0.75)" (m: 0 or natural number), to supply a signal to undergo the filter processing based on a signal having phase difference "π" from the sampled signal, from the signal generation means to the switched capacitor filter means, thereby allowing a demodulated signal to be output from the switched capacitor filter means.

7. The demodulation circuit according to claim 6, wherein the demodulation control means drives the sampling means to sample the modulated signal with its polarity being inverted or drives the signal generation means to generate a signal to undergo the filter processing with its polarity being inverted, thereby matching polarity of the signal supplied to the switched capacitor filter means.

8. The demodulation circuit according to claim 6, wherein if the polarity of signal to undergo the filter processing, said signal being supplied to the switched capacitor filter means, is inverted, the

demodulation control means drives the switched capacitor filter means to perform the filter processing by using the supplied signal with the inverted polarity.

9. The demodulation circuit according to claim 6, wherein the signal generation means is constituted of a unity gain sample buffer.

10. A receiving set comprising:

sampling means for sampling a received signal or an intermediate frequency signal generated on the basis of the received signal;

signal synthesis means for synthesizing and holding the signals sampled by the sampling means;

polarity adjustment means for matching polarities of the signals synthesized by the signal synthesis means, with each other; and

demodulation control means for driving the sampling means to sample the received signal or the intermediate frequency signal at a frequency of the received signal or the intermediate frequency signal multiplied by "1/(m+0.25)" or "1/(m+0.75)" (m: 0 or natural number) and also driving the signal synthesis means to synthesize and hold the signals having phase difference "π" from each other, thereby allowing a demodulated signal of the received signal or the intermediate frequency signal to be generated by the signal synthesis means.

11. A receiving set comprising:

sampling means for sampling a received signal or an intermediate frequency signal;

switched capacitor filter means;

signal generation means for generating a signal on which the switched capacitor filter means performs filter processing, based on the signal sampled by the sampling means; and

demodulation control means for driving the sampling means to sample the modulated signal at a frequency of the modulated signal multiplied by "1/(m+0.25)" or "1/(m+0.75)" (m: 0 or natural number), to supply a signal to undergo the filter processing based on a signal having phase difference "π" from the sampled signal, from the signal generation means to the switched capacitor filter means, thereby allowing a demodulated signal to be output from the switched capacitor filter means.

12. The receiving set according to claim 11, further comprising signal conversion means for converting said demodulated signal output from the switched capacitor filter means into a digital signal,

wherein the demodulation control means sets a sampling frequency at the sampling means to a switching frequency of the switched capacitor filter means multiplied by "p" or "1/p" (p: natural number), the switching frequency of the switched capacitor filter means to a clock frequency of the signal conversion means multiplied by "q" or "1/q" (q: natural number), and the clock frequency of the signal conversion means to "r times" (r: natural number) a symbol rate determined by a modulation scheme employed by the received signal or the intermediate frequency signal.